Alex Li

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Education

University of Waterloo | *BASc, Computer Engineering* | *University of Waterloo President's Scholarship* | *CGPA: 3.96/4.00 (91%)*
- Relevant Courses: Programming in C++, Digital Logic, Circuits, Discrete Math, Linear Algebra, Calculus

Technical Skills

Languages: Python, Java, C, C++, C#, JavaScript, TypeScript, SQL, HTML/CSS, Verilog, TCL
Frameworks: Next.js, Node.js, Express.js, React.js, Django, FastAPI, Flask, Tailwind CSS, React Native, Expo, Unity, Jinja2
Libraries: SQLModel, SQLAlchemy, Pydantic, OpenCV, YOLOv3, ElevenLabs, PyTorch, Meta XR SDK, OpenXR
Embedded: Altera MAX10 FPGA, Intel Quartus Prime, ModelSim, Arduino UNO R4 Minima, UART, NeoPixel, HC-SR04, RTC, PWM
Developer Tools: Pytest, Git, GitHub, Linux, Vercel, Jupyter

Experience

Software Developer | *UW Orbital* | *Waterloo, Ontario, Canada* Aug. 2025 – Present
- Reduced average debugging time by **40%** by introducing middleware with request tracing and centralized error handling
- Engineered **12+** REST API endpoints for satellite command objects using FastAPI with Pydantic validation and SQL storage
- Achieved **95%** code coverage by developing a Pytest test suite with **50+** unit tests for endpoint verification in CI/CD pipeline

Software Developer | *UW Reality Labs* | *Waterloo, Ontario, Canada* Aug. 2025 – Present
- Implemented VR hand pose recognition using **3** AND-gated recognizers to detect closed-fist gestures across **2** hands
- Built a grab interaction system with **4** Meta SDK interactor components, enabling pinch-based object manipulation in VR
- Trained a **3-layer** feedforward neural network in PyTorch on **100,000** RGB samples over **1,000** epochs for binary classification

Computer Architecture Research Intern | *CEcloud* | *Beijing, China* Jun. 2025 – Aug. 2025
- Benchmarked virtual memory management across **3** OS architectures using **8** CPU/GPU workload configurations
- Identified **15-25%** latency variance across CPU/GPU workloads by analyzing paging behavior and page table performance
- Delivered a **45-minute** technical presentation on memory management trade-offs to **20+** researchers and engineers

Web Development Intern | *Tsinghua University* | *Beijing, China* Jun. 2024 – Aug. 2024
- Decreased user-reported issues by **30%** by overhauling UI styling across **15+** pages for WCAG accessibility compliance
- Improved page load performance by **20%** by refactoring CSS for an academic website serving **500+** monthly users
- Drove weekly design reviews with **2** teammates, iterating on usability improvements based on user feedback data

Projects

TrueLight | *Python, JavaScript, TypeScript, Next.js, Node.js, FastAPI, React Native, Expo, OpenCV, YOLOv3, ElevenLabs, HTML/CSS*
- Architected a cross-platform accessibility app providing real-time object detection and audio alerts for **6** color vision profiles
- Achieved under **500ms** end-to-end response time using FastAPI with YOLOv3-tiny inference and OpenCV color analysis
- Shipped **50** commits in a **24-hour** hackathon, coordinating frontend-backend integration with a team of **4** developers

Data Structures Library | *C++*
- Implemented **6** core data structures (DynamicArray, LinkedList, Stack, Queue, HashMap, BST) without using STL containers
- Outperformed std::unordered_map by **12%** on insert/get operations via efficient hash function and collision handling
- Validated correctness with **50+** assert-based unit tests using randomized inputs of up to **3,000,000** elements

Study Planner | *Python, SQL, Flask, SQLAlchemy, HTML/CSS, Jinja2*
- Developed a full-stack Flask app with SQL database to manage academic tasks with **7** metadata fields per task
- Implemented **3** filtered views (all, upcoming, overdue) and **4** persistent sorting options to prioritize task subsets
- Designed a responsive CSS layout with visual status highlighting to ensure usability across various devices and browsers

FPGA Arithmetic Logic Unit | *Verilog, TCL, Altera MAX10 FPGA, Intel Quartus Prime, ModelSim*
- Designed a **4-bit** ALU supporting **4** logic operations (AND, OR, XOR, XNOR) using structural Verilog with MUX-based selection
- Implemented a **4-bit** ripple-carry adder and a **7-segment** decoder displaying **16** hex patterns on dual **7-segment** displays
- Verified functionality via ModelSim waveform simulations across **8+** test cases and deployed to the Altera MAX10 FPGA

CircadiaSense | *C++, Arduino UNO R4 Minima, UART, NeoPixel, HC-SR04, RTC, PWM*
- Developed an automated circadian lighting system with smooth color transitions across **3** modes to improve patient sleep
- Implemented gesture-based brightness control via HC-SR04, mapping distance to LED intensity with smoothing algortihms
- Achieved **10%** faster sleep onset by integrating **4** hardware components (Arduino, LCD, LED strip, sensor) with a team of **4**